Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in this application.

Listing of Claims:

Claim 1 (Previously Presented): A semiconductor device, comprising:

a main conductor layer having an end that is electrically connected to an electrode pad;

an insulating layer having an opening section on said main conductor layer; and

a protrudent electrode electrically connected to said main conductor layer via said opening section, said protrudent electrode being made of Sn or a metal having Sn as its main component,

said semiconductor device further comprising:

a metal layer completely covering a bottom surface, but not completely covering side surfaces, of the opening section on the main conductor layer so that said metal layer is provided between said main conductor layer and said protrudent electrode, wherein

said metal layer includes a nickel layer and a gold layer,

said nickel layer is made of Ni or a metal having Ni as its main component, by electroless plating; and

said gold layer is made of Au or a metal having Au as its main component.

Claims 2-4 (Canceled).

Claim 5 (Previously Presented): The semiconductor device as set forth in Claim 1, wherein said gold layer has a thickness ranging from 0.003 μm to 1 μm.

Claim 6 (Original): The semiconductor device as set forth in Claim 1, wherein said protrudent electrode is formed so that said protrudent electrode has a part, which protrudes from said opening section, of a size greater than an area of said opening section.

Claim 7 (Original): The semiconductor device as set forth in Claim 1, wherein said main conductor layer is made of Cu or a metal having Cu as its main component.

Claims 8 and 9 (Canceled).

Claim 10 (Previously Presented): The semiconductor device as set forth in Claim 1, further comprising:

a foundation metal layer made of Ti, Ti-W, Cr, or a metal having any of those elements as its main component, under said main conductor layer.

Claims 11-16 (Canceled).

Claim 17 (Previously Presented): A semiconductor device, comprising:

a conductive wiring layer connected to an electrode pad formed on a semiconductor substrate;

an insulating layer formed on the wiring layer and having an opening therein which exposes an upper surface portion of the wiring layer;

a metal layer completely covering the upper surface portion of the wiring layer exposed by the opening, but not completely covering side surfaces of the opening; and

a protruding electrode electrically connected to the wiring layer via the metal layer, the protruding electrode being made of Sn or a metal having Sn as its main component, wherein

the metal layer in the opening comprises a barrier metal layer and a top layer, and

the barrier metal layer is formed only in the opening.

Claim 18 (Previously Presented): The semiconductor device according to claim 17, wherein the conductive wiring layer comprises first and second metal layers.

Claim 19 (Previously Presented): The semiconductor device according to claim 18, wherein the first metal layer comprises a barrier metal layer and a metal adhesion layer.

Claim 20 (Canceled).

Claim 21 (Previously Presented): The semiconductor device according to claim 17, wherein the thickness of the top layer is between 0.003 micrometers and 1 micrometer.

Claim 22 (Previously Presented): The semiconductor device according to claim 17, wherein an upper portion of the protruding electrode is wider than the opening formed in the insulating layer.

Claim 23 (Previously Presented): The semiconductor device according to claim 17, wherein the wiring layer is connected to the electrode pad via an opening formed in another insulating layer.

Claim 24 (Previously Presented): The semiconductor device according to claim 23, wherein the other insulating layer comprises an inorganic layer and an organic layer.

Claim 25 (Previously Presented): A semiconductor device, comprising:

a wiring layer connected to an electrode pad formed on a semiconductor substrate;

an insulating layer formed on the wiring layer and having an opening therein which exposes an upper surface portion of the wiring layer;

a metal layer completely covering the upper surface portion of the wiring layer exposed by the opening, but not completely covering side surfaces of the opening; and

a protruding electrode electrically connected to the wiring layer via the metal layer, the protruding electrode being made of Sn or a metal having Sn as its main component,

wherein the wiring layer comprises a first, second and third metal layers,

wherein the metal layer in the opening comprises a barrier metal layer and a top layer, and

wherein the barrier metal layer is formed only in the opening.

Claim 26 (Previously Presented): The semiconductor device according to claim 25, wherein the top layer comprises Au.

Claim 27 (Canceled).

Claim 28 (Previously Presented): The semiconductor device according to claim 25, wherein the insulating layer comprises polyimide resin.

Claims 29 and 30 (Canceled).

Claim 31 (Previously Presented): The semiconductor device according to claim 17, wherein

the top layer comprises a material having good wetting properties with respect to the material which comprises the protrudent electrode.

Claim 32 (Previously Presented): The semiconductor device according to claim 17, wherein

the top layer comprises a material having good wetting properties with respect to the material which comprises the protrudent electrode, and

the barrier metal layer comprises a material preventing interdiffusion of a material comprising the main conductor layer and the material comprising the top layer.

Claim 33 (Previously Presented): The semiconductor device according to claim 25, wherein

the top layer comprises a material having good wetting properties with respect to the material which comprises the protrudent electrode.

Claim 34 (Previously Presented): The semiconductor device according to claim 25, wherein

the top layer comprises a material having good wetting properties with respect to the material which comprises the protrudent electrode, and

the barrier metal layer comprises a material preventing interdiffusion of a material comprising the main conductor layer and the material comprising the top layer.

Claim 35 (Previously Presented): A semiconductor device, comprising:

a conductive wiring layer connected to an electrode pad formed on a semiconductor substrate;

an insulating layer formed on the wiring layer and having an opening therein which exposes an upper surface portion of the wiring layer;

a metal layer having lateral dimensions defined by the size of the opening, the metal layer completely covering the upper surface portion of the wiring layer exposed by the opening, but not completely covering side surfaces of the opening; and

a protruding electrode electrically connected to the wiring layer via the metal layer, the protruding electrode being made of Sn or a metal having Sn as its main component,

wherein the metal layer comprises a barrier metal layer and a top layer.

Claim 36 (New): The semiconductor device according to claim 17, wherein the barrier metal layer is made by electroless plating.

Claim 37 (New): The semiconductor device according to claim 25, wherein the barrier metal layer is made by electroless plating.

Claim 38 (New): The semiconductor device according to claim 35, wherein the barrier metal layer is made by electroless plating.